REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed August 21, 2006. Claims 1-26 were pending in the Application prior to the outstanding Office Action. Claims 11, 16, 17, 22, 24 and 25 are being amended, and claims 1-9, 13 and 19 are being canceled. Claims 10-11, 14-18 and 20-26 remain for the Examiner's consideration. Reconsideration and withdrawal of the rejections are respectfully requested.

I. Drawings

Per the Examiner's request, Applicants are submitting a replacement sheet for FIG. 1, which is now labeled as Prior Art.

II. Claim Objections

Claims 3, 6, 16 and 24 were objected to for minor informalities. The suggested corrections have been made to claims 16 and 24. Claims 3 and 6 have been canceled. Applicants respectfully request that the objections to claims 16 and 24 be reconsidered and withdrawn.

III. Claim Rejections Under 35 U.S.C. § 112

Claim 22 was rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. More specifically, claim 22 was rejected for using the term "register bank", which was alleged to not be a well-known technical term.

A register bank is merely a bank of registers, i.e., a plurality of registers. Accordingly, to expedite prosecution, Applicants have changed the term "register bank" to "a plurality of driver registers." Support for this amendment is provided in the application as originally filed, e.g., in FIG. 2. In view of this Amendment, Applicants respectfully request that this rejection be reconsidered and withdrawn.

IV. Summary of Claim Rejections Under 35 U.S.C. § 102

Claims 1, 2, 5, and 7-13 were rejected 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 5,243,699 to Nickolls et al. (hereafter "Nickolls").

Claims 3 and 4 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nickolls.

Claim 6 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nickolls in view of U.S. Patent No. 6,470,467 to Tomishima et al. (hereafter "Tomishima").

Claims 14 and 16 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nickolls in view of U.S. Patent No. 5,812,881 to Ku et al. (hereafter "Ku").

Claim 15 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nickolls and Ku in view of U.S. Patent No. 4,641,276 to Dunki-Jacobs (hereafter "Dunki-Jacobs").

Claim 17 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nickolls in view of U.S. Patent No. 5,506,825 to Gushima al. (hereafter "Gushima"). It also appears that claims 18-23 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nickolls in view of Gushima

Claim 24 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nickolls and Gushima, in view of Tomishima.

V. Discussion of the Claims

A. Claims 1-9

Claims 1-9 have been canceled without prejudice or disclaimer of the invention therein. Accordingly, the rejections thereof are presently moot.

B. Claim 10

Claim 10 is reproduced below for the convenience of the Examiner.

10. (Original) A method for double buffering serial transfers during a read operation in which a host attempts to read data from a location in a device, comprising:

(a) serially transferring address bits received from the host into an address shift register in the device,

(b) serially transferring data bits present in a data shift register in the device, from the device to the host, wherein the data bits present in the data shift register are associated with a previous read operation;

(c) after completing the serial transfer of the address bits into the address shift register, transferring, in parallel, the address bits into an address holding register in the device, wherein the address bits identify the location, which contains requested data bits; and

(d) after the requested data bits are read from the location into a data holding register, transferring the requested data bits, in parallel, from the data holding register to the data shift register;

wherein the requested data bits will be transferred, serially, from the data shift register to the host the next time the host performs a read operation.

Claim 10 is directed to a unique and unobvious method for double buffering during a read operation, in which a host attempts to read data from a location in a device. Claim 10 was rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Nickolls. However, as explained below, Applicants assert that Nickolls does not teach or suggest claim 10.

For example, Nickolls does not teach or suggest step (b) of claim 10, which involves "serially transferring data bits present in a data shift register in the device, from the device to the host, ***wherein the data bits present in the data shift register are associated with a previous read operation***" (emphasis added). Further, Nickolls does not teach or suggest that "***the requested data bits will be transferred, serially, from the data shift register to the host the next time the host performs a read operation***" (emphasis added), as also required by claim 10.

An explanation of the claimed read operation is provided in paragraphs [0031]-[0033] of Applicants' specification, which are reproduced below for the convenience of the Examiner:

> "**[0031]** It is noted that during read operations, one extra (e.g., dummy) read data cycle is used, since the data holding register 222 delays the read-back data by one read cycle. For example, if the host 102 is reading back four addresses (they do not have to be sequential), the general flow would look like the following:
>
> ```
> Send Address N.
> Read data previously stored in holding register (use
> it or discard it)
> Send Address N+1
> Read Data from Address N
> Send Address N+2
> Read Data from Address N+1
> Send Address N+3
> Read Data from Address N+2
> Send Address N+4
> Read Data from Address N+3
> ```
>
> In other words, five addresses are sent, and five address cycles occur, in order to read four addresses. More generally, in order to read N addresses (which may or may not be sequential), N+1 read cycles are used. However, in many applications (such as in a laser diode driver application) the host 102 seldom reads data using the serial interface, except during testing and debugging. Thus, the extra read cycle does not occur often, except in a non-time critical operation. Also, since the host knows that the data it is reading is delayed by one read cycle, the host may merely wait until a further read cycle is performed to get data that is delayed due to the double buffering.
>
> **[0032]** FIG. 6 is a read operation timing diagram that is useful for further explaining embodiments of the present invention. The host serial controller 202 starts a serial transfer cycle by driving the SEN line HIGH, which will enable the mode and address bits to be clocked by the driver serial controller 212 and appropriately shifted into the address shift register 224. The data already present in the data shift register (e.g., from a previous read operation) will then be serially transferred (e.g., over the SDIO line) from the data shift register 222 to the host

102. When the SEN goes LOW, the address bits in the address shift register 224 will be transferred in parallel to the address holding register 226. These address bits are then used to read the requested data bits (at the location specified by the address bits) into the data holding register 222. These data bits are then transferred in parallel from the data holding register 222 to the data shift register 220. To actually get the data in the data shift register 220, the host must initiate another read cycle so that the this data can get serially shifted to the host (e.g., over the SDIO line).

[0033] Embodiments of the present invention, relating to read operations, can be summarized with reference to FIG. 7. At a step 702, address bits are serially transferred from the host into an address shift register (e.g., 224) in a device (e.g., a laser driver of a storage device). At a step 704, data bits present in a data shift register (e.g., 220) in the device, are serially transferred from the device to the host. These data bits present in the data shift register are associated with a previous read operation. After completing the serial transfer of the address bits into the address shift register, the address bits are transferred in parallel into an address holding register (e.g., 226) in the device. These address bits identify the source location (e.g., register or memory location), which contains the requested data bits. At a step 706, after the requested data bits are read from the source location into a data holding register (e.g., 222), the requested data bits are transferred in parallel from the data holding register to the data shift register (e.g., 220). The requested data bits will then be transferred, serially, from the data shift register to the host the next time the host performs a read operation. Thus, if the host needs that data immediately (yet does not need to read additional data at the time), the host may perform a dummy read operation to thereby cause that data to get serially transferred to the host."

In the Office Action, with regards to step (b) of Applicants' claim 10, it was alleged that lines 58-60 of Nickolls' claim 10 make it "readily apparent that the data [serially transferred from a data shift register of a device to a host] is associated with the address given in the previous operation". Applicants respectfully disagree, for at least the following reasons.

Lines 58-60 of Nickolls' claim 10 say that a data register comprises "a data shift register for engaging in serial transfer of data with the serial bus through a serial port, and for engaging in parallel transfer of data through a parallel port". This language of Nickolls merely states that a data register can be used for both serial and parallel data transfers. However, there is absolutely no teaching or suggestion in this portion of Nickolls, nor any other portion of Nickolls, that during a read operation the data being serially transferred from a data shift register (in a device) to a host are associated with a previous read operation, as is required by Applicants' claim 10.

Further, Nickolls relates to a system that includes "thousands" of processor elements (PEs) that are connected to a few I/O devices (see column 4, lines 63-66). Because of this, it would not make sense for Nickolls to have a processor element that is performing a read operation to have to wait for a next read cycle to obtain its requested data. Rather, it is most likely that a processor element in Nickolls would have to complete the serial transferring of data being read, before that processor or another processor were to perform another read operation using the same serial bus, as would normally be the case. In other words, it is more likely that in Nickolls, during a read operation, the data bits present in a data shift register are associated with a present (not the next) read operation; and that requested data bits are serially transferred from the data shift register to the host the present (not the next) time the host performs the read operation.

In the types of applications within with the claimed invention may be used (such as in a laser diode driver application) the host seldom reads data using the serial interface, except during testing and debugging (as explained in paragraph [0031] quoted above). Thus, the extra read cycle does not occur often, except in a non-time critical operation. Also, since the host knows that the data it is reading is delayed by one read cycle, the host may merely wait until a further read cycle is performed to get data that is delayed due to the double buffering (as also explained in paragraph [0031] quoted above).

Although not exactly stated in the rejection of claim 10 (but stated in the rejections of claim 13 and 19, which include similar features), it appears that the Examiner may be asserting that Nickolls **inherently** teaches "serially transferring data bits present in a data shift register in the device, from the device to the host, wherein the data bits present in the data shift register are associated with a previous read operation" and that "the requested data bits will be transferred, serially, from the data shift register to the host the next time the host performs a read operation". As explained below, Applicants respectfully assert that Nickolls does not inherently teach such claimed features.

As stated in MPEP § 2112.IV, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir.

1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " As also explained in MPEP § 2112.IV, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

When stating that the features of original claims 13 and 19 were inherently taught by Nickolls, the Examiner did not explain why Nickolls must perform serial transfers during a read operation as claimed. Rather, the statement in the Office Action that Nickolls inherently teaches such features was conclusory and without support. When rejecting claims 13 and 19, the Examiner went on to say that "this rejection can further be enforced by the disclosure on col. 2, lines 21-25 of Nickolls et al." However, col. 2, lines 21-25 of Nickolls, merely states that "active processors have the autonomy to read or write data at any target address in the I/O stream buffer, rather than being assigned a fixed mapping onto the file." This simply means that processors of Nickolls are not limited as to which address in a buffer the processors can read from or write to. This statement has nothing to do with data bits being transferred from a data holding register to a host during a read operation being associated with a previous read operation, which is required by claim 10 (as well as by original claims 13 and 19).

Further, it is pointed out that the European (EU) Patent Examiner agreed that claim 10 is patentable, as can be seen in the EPO Written Opinion (a copy of which is attached hereto, and a copy of which was previously submitted with the IDS filed on March 8, 2005). More specifically, in the EPO Written Opinion, the EU Patent Examiner stated that "Claim 10 is characterized in transferring the requested data bits, serially, from the data shift register to the host the next time the host performs a read operation." The

technical problem, as characterized by the EU Examiner was "how to enhance the access speed at a sequence of consecutive read requests". Further, in stating that the claimed solution was inventive, the EU Examiner stated the following:

> "The general subject-matter of pipelining memory access (read) requests is known (see D2). However within the context of a serial memory access a requesting device needs to know the exact point of time at which the requested data is available in order to receive said data. On obvious solution would be to count clock cycles in the requesting device. A requesting device according to the invention of claim 10 does not need such a clock cycle counting function as it knows that right when starting the next read operation it is supposed to start receiving the data of the previous request. As a disadvantage the requesting device when sending a single request or a last request of a sequence must send a further dummy request in order to receive the data of the single or last request. The solution of claim 10 is thus considered not obvious."

For the various reasons set forth above, Applicants assert that Nickolls does not explicitly or inherently teach or suggest "serially transferring data bits present in a data shift register in the device, from the device to the host, wherein the data bits present in the data shift register are associated with a previous read operation", and that "the requested data bits will be transferred, serially, from the data shift register to the host the next time the host performs a read operation", as required by claim 10. Further, Applicants respectfully assert that the other cited prior art references do not teach or suggest such deficiencies of Nickolls. Accordingly, Applicants respectfully request that the 102(b) rejection of claim 10 be reconsidered and withdrawn.

C. Claims 11-16

Claim 11 has been amended to include the features of original claim 13, which has accordingly been canceled (because its features are now in claim 11). More specifically, claim 11 has been amended to state that "during a read operation, data bits transferred from the data holding register to the host, are associated with a previous read operation."

In the Office Action (in the rejection of original claim 13), it was alleged that this feature "it is an inherent feature in Nickolls et al. that during a read operation, data bits transferred from the data holding register to the host, are associated with a previous read operation since the address is required in order for the system to specifically retrieved the

requested data since a read operation is supposed to retrieved the data that is requested, which is corresponding to the data address provided." It is further asserted in the Office Action that "this rejection can further be enforced by the disclosure on col. 2, lines 21-25 of Nickolls et al."

First, with regards to col. 2, lines 21-25 of Nickolls, this portion of Nickolls merely states that "active processors have the autonomy to read or write data at any target address in the I/O stream buffer, rather than being assigned a fixed mapping onto the file." This simply means that processors of Nickolls are not limited as to which address in a buffer the processors can read from or write to. This statement has nothing to do with data bits being transferred from the data holding register to the host during a read operation being associated with a previous read operation, which is required by claim 11.

Second, with regards to the statement that Nickolls inherently teaches these features, Applicants respectfully disagree. As explained above, in the discussion of claim 10, it is more likely that a processor element in Nickolls would have to complete the serial transferring of data being read, before that processor or another processor were to perform another read operation using the same serial bus, as would normally be the case. In other words, in Nickolls it is more likely that during a read operation, data bits transferred from the data holding register to the host, are associated with a present (not previous) read operation. Further, as explained above in the discussion of claim 10, MPEP § 2112.IV requires that it be clear that the missing matter in the prior art must necessarily be present in the prior art and so recognized by persons of ordinary skill. Inherency, may not be established by probabilities or possibilities. Further as explained above in the discussion of claim 10, MPEP § 2112.IV also states that when "relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

For reasons just set forth above, and for many of the same reasons set forth in the discussion of claim 10, Applicants respectfully assert that Nickolls does not inherently or explicitly disclose or suggest that "during a read operation, data bits transferred from the data holding register to the host, are associated with a previous read operation." Further,

Applicants assert that the other applied prior art, alone or in combination, do not teach such deficiencies of Nickolls.

For at least the reasons set forth above, Applicants respectfully request that the 102(e) rejection of claim 11, as amended, be reconsidered and withdrawn.

Claims 12 and 14-16 depend from and add additional features to claim 11. For at least the reason that these claims depend from claim 11, Applicants believe that these claims are also patentable over the cited prior art.

D. Claims 17-24

Claim 17 has been amended to include the features of original claim 19, which has accordingly been canceled (because its feature are now in claim 17). More specifically, claim 17 has been amended to state that "during a read operation, data bits transferred from the data holding register to the host, are associated with a previous read operation." For at least reasons similar to those discussed above with regards to claim 11, Applicants respectfully assert that claim 17, and its dependent claims 18 and 20-24, should be allowable over the applied prior art.

VI. Allowable Subject Matter

Applicants thank the Examiner for indicating the claims 25-26 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 25 has been amended to be in independent form, as suggested. Accordingly, it is respectfully requested that claim 25 and its dependent claim 26 be allowed.

VII. Conclusion

In light of the above, it is respectfully requested that all outstanding rejections and objections be reconsidered and withdrawn. The Examiner is respectfully requested to telephone the undersigned if he can assist in any way in expediting issuance of a patent.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this reply, including any fee for extension of time, which may be required.

Respectfully submitted,

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